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<input type="checkbox"/> Response to Missing Parts/Incomplete Application	Certified copy of European Patent Office patent application 02368081.2, filed 07/24/2003 in US	
<input type="checkbox"/> Response to Missing Parts under 37 CFR 1.52 or 1.53	Priority date: 7/26/02	

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Patentanmeldung Nr. Patent application No. Demande de brevet n°

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Sheet 2 of the certificate
Page 2 de l'attestation**

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Armonk, NY 10504
UNITED STATES OF AMERICA

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Titre de l'invention:
An improved differential amplifier with DC offset cancellation

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AN IMPROVED DIFFERENTIAL AMPLIFIER WITH DC OFFSET CANCELLATION

5 FIELD OF THE INVENTION

The present invention relates to large bandwidth high frequency amplifiers to be placed in the receiver section of a high speed transmission system and more particularly to an improved differential amplifier provided with a parallel
10 feedback loop to amplify high frequency signals wherein the DC offset is significantly reduced and the input impedance matching improved.

BACKGROUND OF THE INVENTION

In the receiving part of high speed wired transmission
15 systems (like Ethernet), there is a need for the amplification of high frequency low power signals. This is achieved with a dedicated differential amplifier basically consisting of a chain of low gain large bandwidth amplifiers with a parallel feedback loop, usually called post-amplifier or PA, that is
20 placed after the optical circuitry (photodiode and associated transimpedance circuit) of the receiving section.

The block diagram of such a conventional amplifier is shown in FIG. 1. Now turning to FIG. 1, the conventional differential amplifier referenced 10 is comprised of an input
25 matching circuit 11, an amplification section 12 consisting of a chain of large bandwidth amplifiers to obtain enough gain in the frequencies of interest (in the GHz range) and finally a circuit block 13 in the DC feedback loop connected in parallel between the inputs and outputs of said amplification section
30 12. All these circuit components are mounted in a differential manner. As apparent in FIG. 1, input matching circuit 11

consists of a single resistor for the sake of simplicity, that is mounted in parallel between two input terminals 14 and 15 receiving single-ended input signals IN_p and IN_n respectively from a preceding stage schematically represented by a voltage supply V_{in} and a resistor R . V_{in} will be referred to hereinbelow as the input voltage for the sake of simplicity. Corresponding single-ended output signals OUT_p and OUT_n are available at output terminals 18 and 19 respectively, and likewise define the output signal V_{out} , such as $V_{out} = V_{OUT_p} - V_{OUT_n}$.

Feedback block 13 includes an amplifier 16 (for further amplification of the output signal V_{out}) and a RC network 17 comprised of blocks 17' for low pass filtering and 17'' to perform the summation of the direct input and feedback signals at nodes A and B at the inputs of the first amplifier of amplification section 12 as shown in the drawing. The dotting which is made at nodes A and B allows the desired reduction of the DC offset by the single-ended feedback signals F_{bn} and F_{bp} . As known for the skilled professional, the voltage V at the inputs of the amplification section 12 is a function of V_{in} and V_{fb} , where $V_{fb} = V_{FB_p} - V_{FB_n}$. Note that a quite similar circuit is described in the article: "622Mb/s CMOS limiting amplifier with 40 dB dynamic range" by T. Yoon & B. Jalali, published in Electronics Letters, Sept. 26th, 1999, Vol. 32 No 20, pp 1920-1921.

The conventional differential amplifier shown in FIG. 1 only partially reduces the DC offset, because, unfortunately, it amplifies not only the useful input signal but also any DC offset signal, coming from the previous circuits or internally generated at the input terminals of amplifier 10. The amplitude of this DC offset signal can be of the same order of magnitude or even greater than the one of the input signal itself and then can detrimentally saturate the differential output signal V_{out} with invalid information. In addition, the feedback block 13, which connects the RC network 17 in parallel on the input matching circuit 11 significantly degrades the

input impedance matching, referred to as the scattering parameter S_{11} in the technical literature.

SUMMARY OF THE INVENTION

According to the present invention there is described a solution to this problem, consisting of an improved large bandwidth high frequency amplifier wherein the DC offset in the output signal is significantly reduced. This is performed by separating the useful high frequency input signal information from the DC offset signal. To that end, a direct and feedback signal combining block is inserted that bridges the direct amplification line and the feedback loop at the summing nodes. As a result, the filtering of the AC components of the output signal that is combined with the input signal is improved. In essence, the direct and feedback signal combining block is comprised of two circuits. A first circuit, typically a buffer or an unitary gain differential amplifier is inserted between the input matching circuit and the amplification section to isolate the input signal from the summing nodes. A second circuit, consisting of a differential amplifier connected to the summing nodes, is inserted in the feedback loop to isolate the feedback block from said nodes and amplifies the feedback signal V_{fb} if necessary. The role of these two circuits is to modify the signal combination at the summing nodes.

In addition to this DC offset signal reduction, the improved amplifier of the present invention offers other outstanding advantages. Because, there the feedback signal does not interfere with the input signal, an excellent input impedance matching is obtained, i.e. the scattering parameter S_{11} is negative and close to infinite. This is mandatory in high speed systems to achieve a low eye-diagram closure or good jitter (and bit error rate) performance. The efficiency of offset reduction can be adjusted and is independent of input signal amplification. The loop stability is ensured by construction. Finally, all elements can be integrated in a

chip using conventional integrated circuit technologies, saving board space, element count and cost.

It is therefore a primary object of the present invention to provide an improved large bandwidth high frequency differential amplifier having a feedback loop that allows to significantly reduce the DC offset.

It is another object of the present invention to provide an improved large bandwidth high frequency differential amplifier having a feedback loop wherein the feedback signal does not interfere with the input signal improving thereby the input impedance matching (represented by the S_{11} parameter).

The novel features believed to be characteristic of this invention are set forth in the appended claims. The invention itself, however, as well as other objects and advantages thereof, may be best understood by reference to the following detailed description of an illustrated preferred embodiment to be read in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 shows a conventional large bandwidth high frequency differential amplifier circuit designed with a parallel feedback loop.

FIG. 2 shows the improved large bandwidth high frequency amplifier basically deriving from the FIG. 1 circuit but provided with an innovative input and feedback signal combining block according to the present invention.

FIG. 3 shows the small signal frequency responses of the FIG. 1 and FIG. 2 amplifier circuits with and without feedback.

FIG. 4 shows a typical implementation of the innovative combining circuit of FIG. 2 in an advanced Bi-CMOS technology.

DESCRIPTION OF A PREFERRED EMBODIMENT

Like reference numerals (with prime) are used through the several drawings to designate identical (corresponding) parts.

The improved large bandwidth high frequency amplifier of the present invention is shown in FIG. 2 where it bears numeral 20. In essence, it differs from the conventional FIG. 1 amplifier 10 by the input and feedback signal combining block 5 that bridges both the direct amplification line and the feedback loop, while the other elements remain substantially identical. Now turning to FIG. 2, the signal and feedback signal combining block referenced 21 is comprised of a circuit 22, typically a buffer or a unitary gain amplifier (as shown 10 in the drawing), placed between the input matching circuit 11 and the amplification section 12 on the one hand, and of a differential amplifier 23 connected in series with the feedback block now referenced 13' because the RC network 17 shown in FIG. 1, can be simplified in some extent (the 15 resistors composing sub-network 17" are no longer necessary). Signals Fbp and Fbn output by feedback block 13' can be amplified in amplifier 23 if necessary, then applied to the summation nodes, now referenced A' and B', respectively. The main role of circuits 22 and 23 is thus to isolate the input 20 signal V_{in} and the feedback signal V_{fb} from these summing nodes. In addition, circuit 23 can be used to amplify the feedback signal V_{fb} .

The relationship between signals at the inputs of the amplification section 12 is substantially the same but 25 circuits 22 and 23 which respectively isolate summing nodes A' and B' from input signal V_{in} and feedback signal V_{fb} at the inputs of the amplification section 12, totally avoid any degradation of the input impedance matching. As a consequence, circuit 22 can accommodate any type of matching circuit 11 30 since there is no more direct connection with the feedback block 13' elements. The response of the feedback loop can also be better controlled and has a full efficiency, whereas in the conventional solution, the matching circuit 11 degrades the gain of the feedback loop and thus its efficiency.

The small signal frequency responses of the conventional and improved amplifiers 10 and 20 are shown in FIG. 3. Curve 30 represents the response of both amplifiers 10 and 20 when there is no feedback loop. Curve 31 represents the response of amplifier 10 which clearly shows that only a partial offset compensation is obtained. Curve 32 represents the response of amplifier 20 when the combining block 21 is implemented. As apparent in FIG. 3, the low frequency response is modified. The DC gain is substantially different from the AC gain (high frequency gain). The two poles F1p and F2p which define the DC and AC gain regions need to be spaced as much as possible, so that the DC gain becomes negative, reducing thereby the DC offset. Curve 32 demonstrates that this highly desirable result is obtained with amplifier 20 implementing the present invention.

Typical DC/AC characteristics of the conventional and improved amplifiers 10 and 20 for identical direct line and feedback loop gain, 100 and 10 respectively, and for identical RC networks are given in Table 1 below.

20

Table 1 : DC/AC Comparison

Circuit	DC Gain [dB]	AC Gain [dB]	F1p [Hz]	F2p [Hz]
Conventional	18.8	33.8	5.79k	30.9k
Improved	-26.0	34.0	5.64k	5.64M

The better efficiency that is obtained with the improved amplifier circuit 20 of the present invention is emphasized by the negative value of the DC gain that stays positive with the conventional amplifier 10 which only achieves a partial compensation of the input offset as mentioned above.

Table 2 below allows an easy comparison of the figures of the S_{11} parameter of that are obtained by simulations (assuming ideal block components are used) for the conventional and improved amplifier circuit 10 and 20.

Table 2 : S_{11} Comparison

Design	S_{11} @ 10Hz [dB]	S_{11} @ 1GHz [dB]
Conventional	-1.7	-40.0
Improved	-inf.	-inf.

The figures of the S_{11} parameter of improved amplifier circuit 20 are quite excellent (close to a negative infinite value in dB). It does not suffer from the degradation due to the RC network 17' thanks to the combined isolation provided by both circuits 22 and 23 at low frequencies.

An example of a preferred hardware implementation of the combining block 21 of FIG. 2 in a Bipolar-CMOS technology is shown in FIG. 4, that clearly shows that circuits 22 and 23 can be advantageously merged in a single circuit. The single-ended input signals, i.e. INp and INn, drive the base of two bipolar transistors Q1 and Q2 mounted in emitter follower to form circuit 22, typically a buffer or a unitary gain amplifier. The bias current is provided by transistors Q3 and Q4 that are part of a conventional full current mirror stage (not detailed) with emitter resistors R1 and R2 to improve its efficiency. The base of transistors Q3 and Q4 is connected to a reference voltage Vref. The transistors Q3 and Q4 act as cascode transistors for the feedback signals. The feedback signals Fbn and Fbp drive the gate of two NFETs N1 and N2 connected in parallel to R1 and R2 and working in their linear region ($V_{ds} < V_{gs} - V_t$). Devices Q3, Q4, N1, N2, R1 and R2 form amplifier 23. Signals Xp and Xn that are generated by combining block 21 are applied to the summation nodes A' and B' at the input of the amplification section 12 (not shown).

Using standard notations, a complete small signal analysis of combining circuit 21 gives: $V = V_{in} + K \cdot V_{fb}$, where $V_{fb} = V_{FBp} - V_{FBn}$ and K is equal to $g_{mN} / (g_{mB} + 1/R_e)$, where $g_{mN} = \mu_n \cdot C_{ox} \cdot W/L$ is the NFET transconductance, $g_{mB} = I_c / U_t$ is the bipolar transconductance and finally, R_e is the emitter resistor (R1 or R2). K is thus a function of the width/length (W/L) ratio of the NFETs and can be adjusted independently to

get the necessary amount of feedback to adjust the offset compensation without modifying the input matching circuit 11.

The advantages of this solution are recited below:

1. The DC offset signal is significantly reduced.
- 5 2. The feedback signal does not interfere with the input signal, maintaining thereby an excellent input impedance matching, i.e. parameter S_{11} is close to an infinite negative value. This is mandatory in high speed systems to achieve a low eye-diagram closure or good jitter (and bit error rate) performance.
3. The efficiency of the offset compensation can be adjusted and is independent of input signal amplification.
4. The loop stability is ensured by construction
5. All elements can be integrated in a semiconductor chip
- 15 using conventional IC technologies (saving board space, element count and cost).

In short, the proposed solution ensures a significant offset reduction and thus improves the feedback efficiency. Moreover, it improves the input impedance matching (S_{11} parameter) on the whole tuning range but mainly at low frequencies.

Improved amplifier circuit 20 can be designed in any standard CMOS or bipolar technology. It has been implemented in a prototype of a post-amplifier chip in an advanced BiCMOS technology for 10 Gb/s Ethernet communications. The chip has been manufactured and tested. As far as amplifier 20 was concerned, results were in very good agreement with the performance predicted by the above simulations, as illustrated by Tables 1 and 2.

30 While the invention has been particularly described with respect to a preferred embodiment thereof it should be understood by one skilled in the art that the foregoing and other changes in form and details may be made therein without departing from the spirit and scope of the invention.

CLAIMS

What is claimed is:

1. An improved large bandwidth high frequency amplifier (20)
5 having a feedback loop comprising:
input terminals (14,15) to receive a input signal (Vin);
output terminals (18,19) to supply an amplified differential
output signal (Vout) as a function of the input signal;
an input matching circuit (11), a first isolation circuit
10 (22) and an amplification section (12) that are connected in
series in the direct amplification line, wherein said
amplification section consists of at least one large bandwidth
low gain differential amplifier to generate said amplified
output signal; and,
15 a parallel feedback circuit (13') consisting of a first
amplifier (16), a RC network (17'), and a second isolation
circuit (23) that are connected in series between said output
terminals and the amplification section inputs.
- 20 2. The improved amplifier of claim 1 wherein said first
isolation circuit is either a buffer or an unitary gain
amplifier.
3. The improved amplifier of claim 1 or 2 wherein said second
isolation circuit is an amplifier having a gain ≥ 1 .

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AN IMPROVED DIFFERENTIAL AMPLIFIER WITH DC OFFSET CANCELLATION

ABSTRACT

There is disclosed an improved differential amplifier (20) having a feedback loop that generates an amplified output signal (V_{out}) from an input signal (V_{in}) supplied by a preceding stage. It comprises an input matching circuit (11) connected to said preceding stage, a buffer (22) and an amplification section (12) connected in series in the direct amplification line, a first amplifier (16), a RC network (17') and a second amplifier (23) connected in series in a parallel loop between the outputs and the inputs of the amplification section that generate the feedback signal. The role of said buffer and second amplifier associated in a dedicated direct and feedback signal combining block (21) is to respectively isolate the input signal and the feedback signal from the summing nodes (A' , B') at the amplification section inputs. As a result, the summation of the input signal and the feedback signal is improved, the DC component of the output signal is filtered out in order to significantly reduce the DC offset. In addition, the input impedance matching represented by parameter S_{11} is considerably improved.

FIG. 2

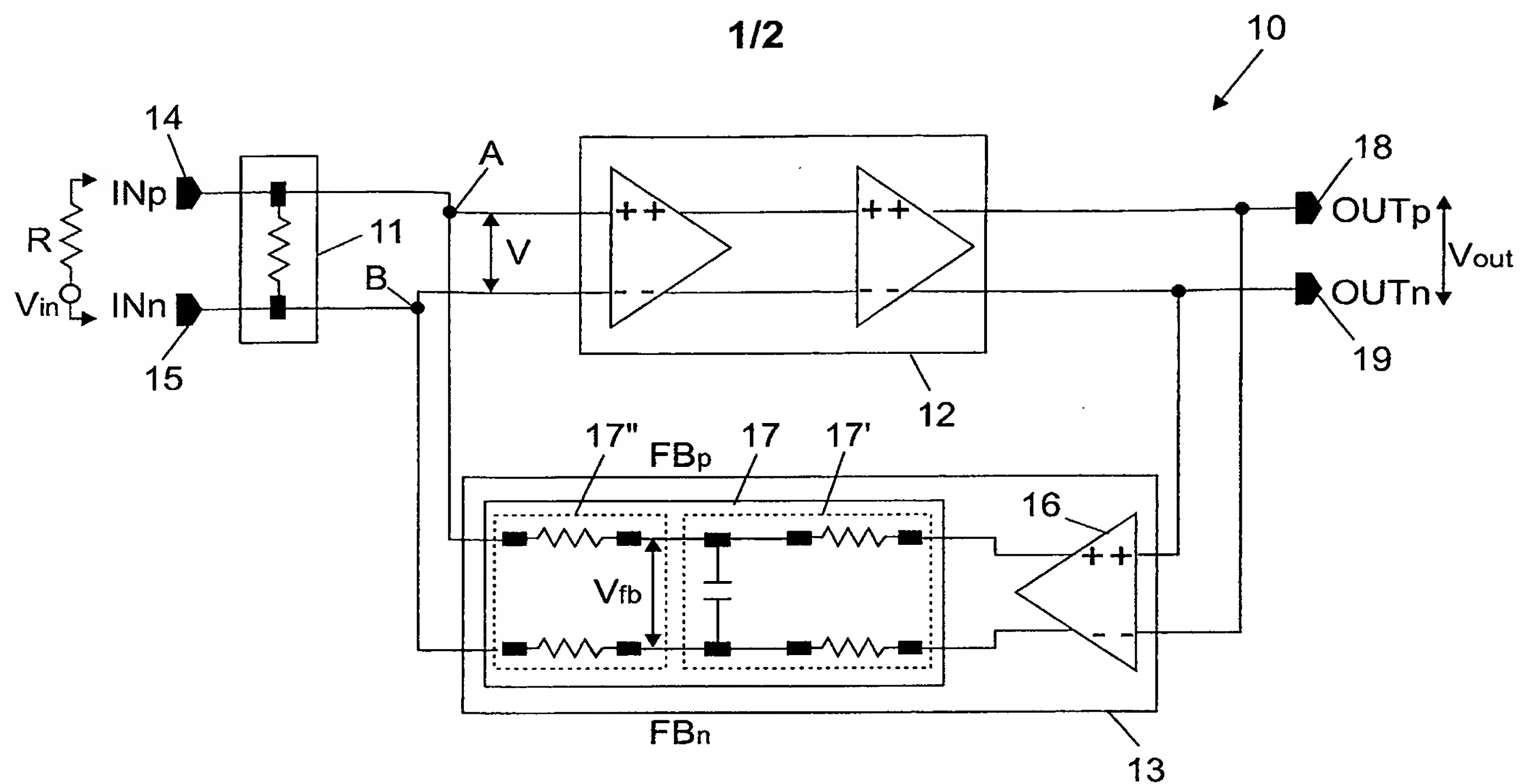


FIG. 1 (Prior Art)

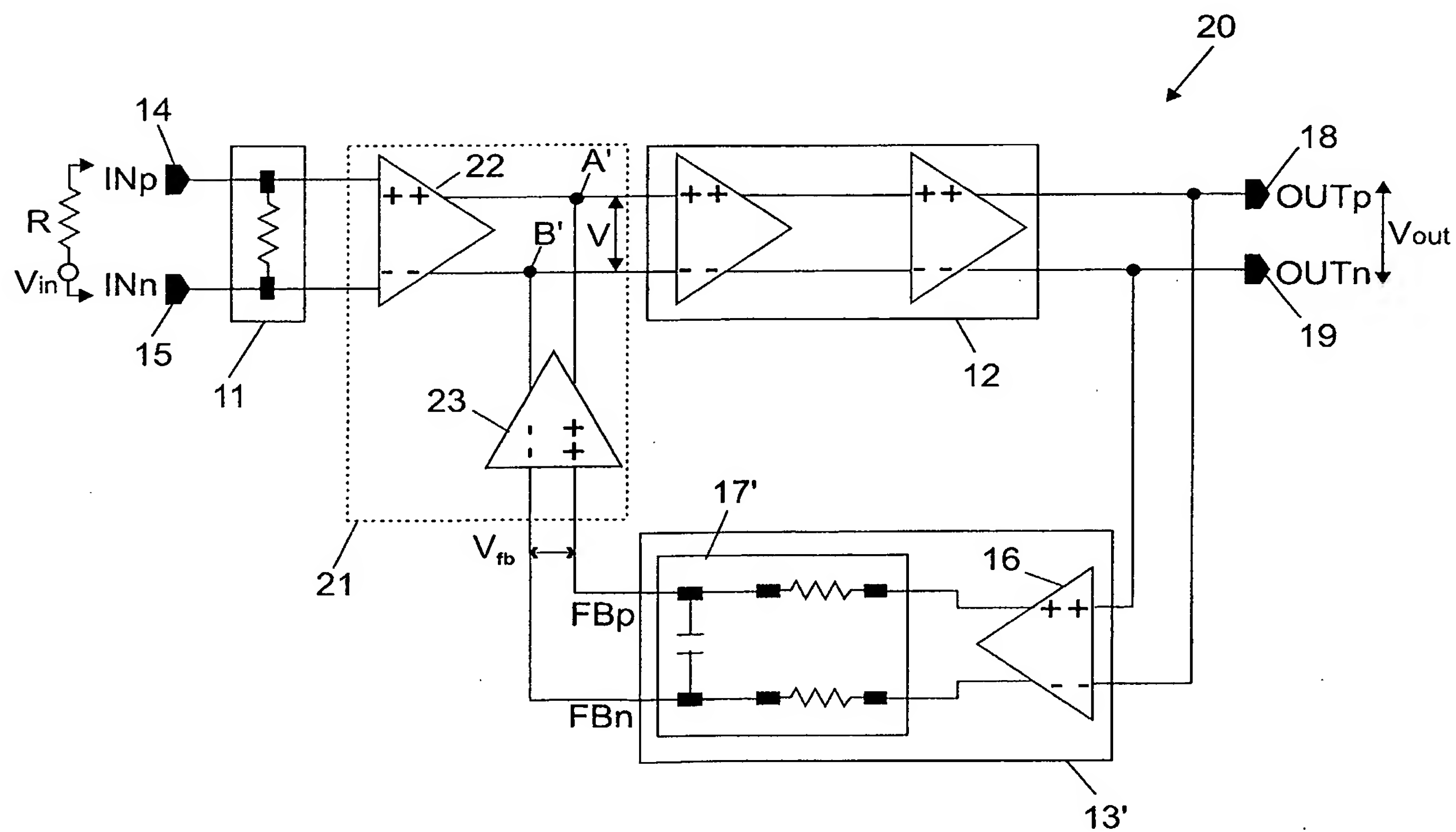


FIG. 2

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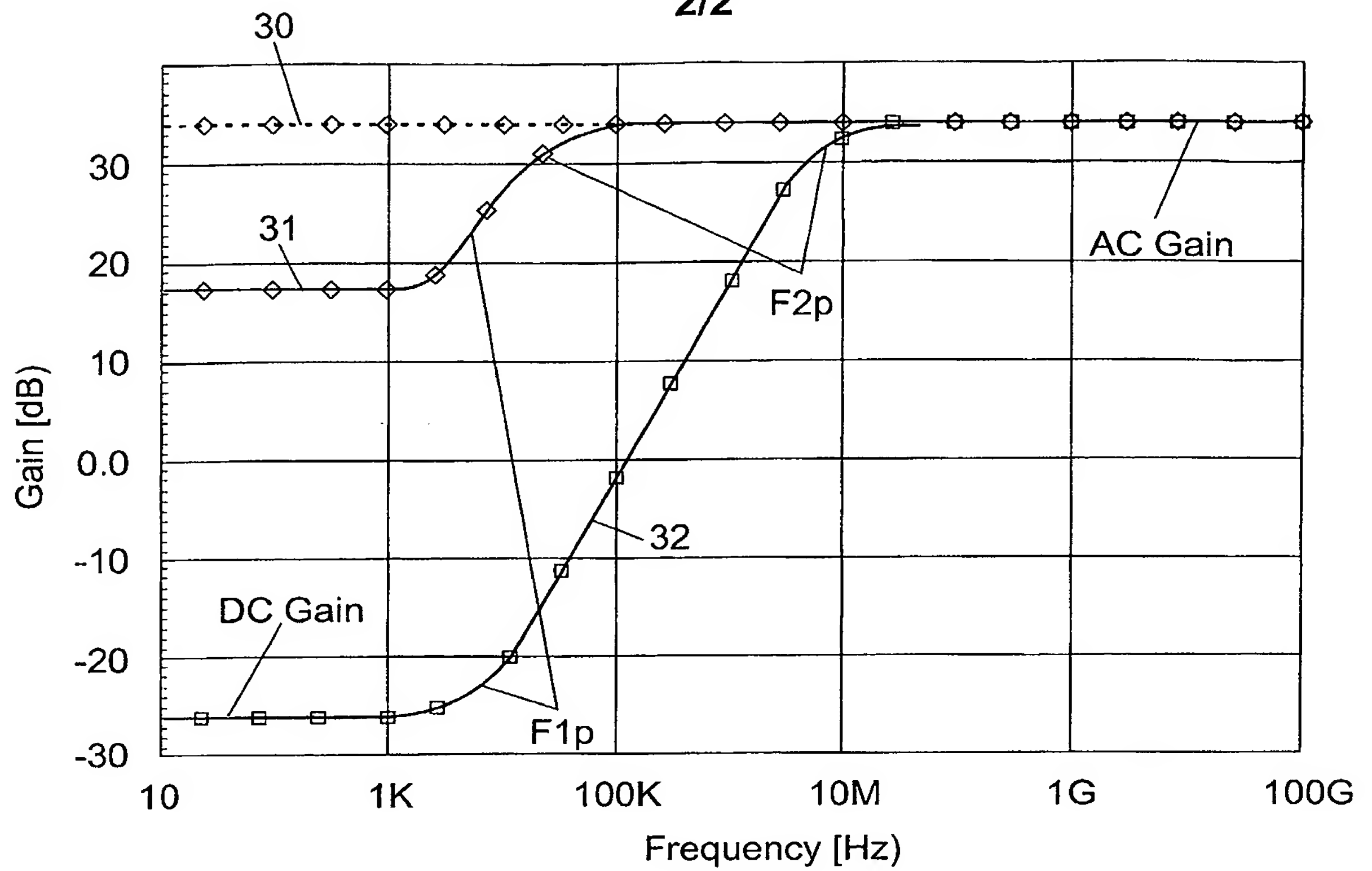


FIG. 3

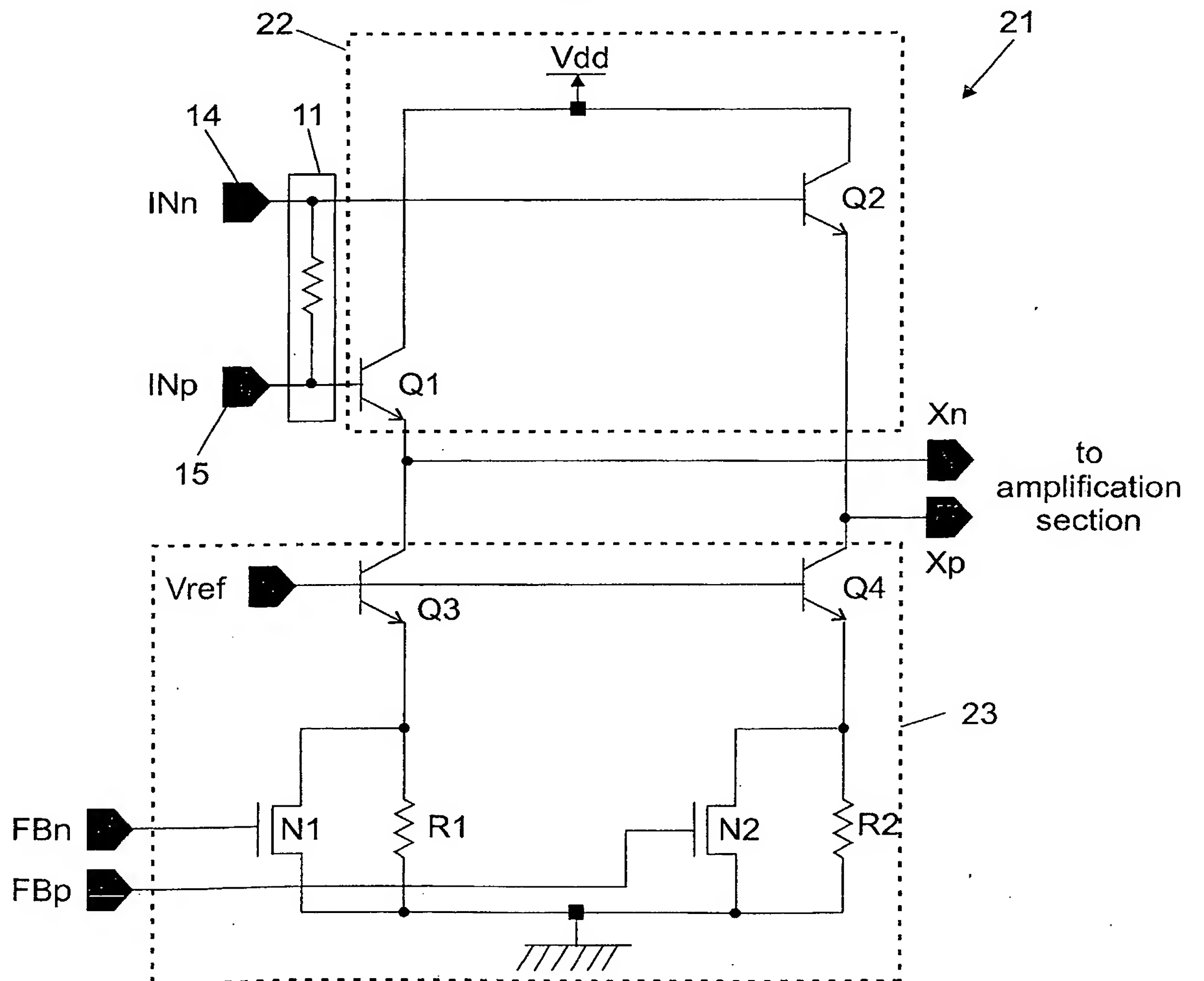


FIG. 4